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EFM32GG995 Errata History

F1024/F512



This document describes known errata for all revisions of EFM32GG995 devices.

1 Errata History

1.1 Errata Overview

Table 1.1 (p. 2) shows which erratum is applicable for each revision. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p0 (www.arm.com) also applies to all revisions of this device.

Table 1.1. Errata Overview

| Erratum ID | rev D | rev C | rev B |
|------------|-------|-------|-------|
| BU1 | | | X |
| BU2 | | | X |
| BU4 | | | X |
| BU5 | X | X | X |
| BU6 | X | | |
| BURTC1 | X | X | X |
| CMU1 | | | X |
| CMU2 | | | X |
| CMU3 | | X | X |
| CMU4 | X | | |
| CMU5 | X | | |
| CUR3 | | X | |
| CUR4 | | X | X |
| EBI1 | | | X |
| EBI2 | | | X |
| EBI3 | X | X | X |
| EMU1 | | | X |

| Erratum ID | rev D | rev C | rev B |
|------------|-------|-------|-------|
| ETM1 | | | X |
| GPIO1 | | | X |
| LES1 | | | X |
| LES2 | | | X |
| LES3 | X | | |
| MSC1 | | X | X |
| OPA1 | | | X |
| PRS1 | X | X | X |
| USART1 | X | X | X |
| USB1 | | | X |
| USB2 | | | X |
| USB3 | X | X | X |
| USB4 | X | X | X |
| USB5 | X | X | X |
| USB6 | | | X |
| USB7 | | X | X |
| USB8 | | X | X |

1.2 EFM32GG995 Errata Descriptions

Table 1.2. EFM32GG995 Errata Descriptions

| ID | Title/Problem | Effect | Fix/Workaround |
|-----|---------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------|
| BU1 | <p>Backup power increased power consumption</p> <p>Additional current consumption on BU_VIN approximately 100uA when</p> | <p>Additional current consumption on BU_VIN approximately 100uA when VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN.</p> | <p>Avoid having VDD_DREG in between 0.3 BU_VIN to 0.7 BU_VIN.</p> |

| ID | Title/Problem | Effect | Fix/Workaround |
|--------|---------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------|
| | VDD_DREG is between 0.3 BU_VIN to 0.7 BU_VIN. | | |
| BU2 | EM4 GPIO retention in backup mode EM4 GPIO retention not shut off in backup mode. | With GPIO retention enabled, GPIO pins will still drive in backup mode. | Do not use EM4 GPIO retention in combination with backup mode. |
| BU4 | EM4 with backup BODs EM4 with backup BODs does not trigger reset. | EM4 with backup BODs does not trigger reset. | Avoid using backup BODs when entering EM4. |
| BU5 | LFXO missing cycles during IOVDD rampings LFXO missing cycles during IOVDD ramping when used in combination with Backup mode. | When IOVDD is ramped, the DC-level of the XTAL signal changes, resulting in missed LFXO cycles and possible glitches on the LFXO clock. | Set PRESC in BURTC_CTRL to greater than 0 when ramping IOVDD in combination with Backup mode to avoid glitches on the LFXO clock. |
| BU6 | Current leakage in Backup mode | In Backup mode, when $VDD > BU_VIN + 0.7$, current will leak from VDD. | To avoid leakage, exit Backup mode before VDD exceeds the voltage where the leakage start by configuring the threshold in EMU_BUACT. |
| BURTC1 | BURTC LPMODE entry Entering LPMODE with LPCOMP=7 causes counter error. | Counting error occurs if overflow on 7 LSBs happens when entering LPMODE with LPCOMP=7. This results in the counter value being 256 less than it should be after the error. The error accumulates. | Avoid using LPMODE with LPCOMP=7. |
| CMU1 | LFxCLKEN write First write to LFxCLKEN can be dropped. | If enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN, then this write can miss its effect. | Make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy. |
| CMU2 | LFXO phase shift Transients on pin D8 cause LFXO phase shift. | Transients on pin D8 can give a temporary phase shift on LFXO. Frequency is unchanged. | No known workaround. |
| CMU3 | LFXO configuration incorrect LFXO configuration incorrect. | For devices with PROD_REV < 15, LFXOBUFCUR in CMU_CTRL is default 0 and LFXOBOOST in CMU_CTRL is default 1. However, these values are incorrect. | On devices with PROD_REV < 15, change LFXOBUFCUR to 1 and LFXOBOOST to 0. |
| CMU4 | LFXO boost buffer current setting | LFXO will not work properly with LFXOBUFCUR in CMU_CTRL set. | Do not set LFXOBUFCUR in CMU_CTRL. |

| ID | Title/Problem | Effect | Fix/Workaround |
|------|-------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | LFXO boost buffer current must be disabled | | |
| CMU5 | LFXO startup at high temperature LFXO does not start at high temperature with default configuration. | For devices with PROD_REV = 16, LFXO may have startup issues with low capacitance crystals when using the default LFXO configuration. | Make this line of code part of your startup code, typically in the start of main(): <code>*((volatile uint32_t*) 0x400c80C0) = *((volatile uint32_t*) 0x400c80C0) & ~(1<<6) (1<<4);</code> . |
| CUR3 | Increased EM2 current Increased consumption in EM2 | Current consumption in EM2 and EM3 has two stable states, the normal state (1200 nA and 900 nA for EM2 and EM3 respectively) and an error state. In the error state the current consumption in EM2 and EM3 is typically 4.5 uA at 25C (manufacturing test limits is set to 7 uA) but will increase with increased temperature. At 85C the error state EM2 and EM3 current consumption is typically 25 uA. It is unpredictable which state the device will go into on EM2/EM3 entry and it can also change state during operation. | No known workaround. |
| CUR4 | Increased current on AVDD2 Increased current on AVDD2 related to VREGO | When VREGO is floating or 0 V, a leakage can appear on AVDD2. This leakage is typically less than 10 uA, but can also rise to around 300 uA. | Make sure VREGO is always defined high when there is power on AVDD2. For bus-powered devices this is always the case, but for devices where the power on VREGO can be lost during operation, e.g. a USB device where the USB phy is powered from VBUS when a master is attached, a 5 MOhm to VDD can help keep VREGO defined. |
| EBI1 | EBI masking functionality EBI masking functionality is not limited to bank selected for TFT. | EBI masking functionality is not limited to the bank selected for TFT (by BANKSEL field in EBI_TFTCTRL). When masking is enabled, a mask match can be generated and suppress writes to any bank. | Disable masking when doing writes that should not be affected. |
| EBI2 | EBI access fails Certain EBI accesses via the Cortex and Debug interface do not work. | Any access from the Cortex to the EBI not aligned to its size does not work. Also, only word accesses from the debug interface works. | Make sure all accesses via the Cortex are aligned to its size, and that all debug accesses are word accesses. |
| EBI3 | Page mode read in D16A16ALE mode Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses. | Page mode read in D16A16ALE mode skips RDSETUP stage for page mode accesses, making the read process go directly from ADDRSETUP to RDPA. | To compensate for the missing hold time related to the ALE address latch, the HALFALE field in EBI_ADDRTIMING can be enabled providing a 1/2 cycle hold time. |
| EMU1 | Debug unavailable during DMA processing from EM2 | DMA requests from LESENSE and the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the | Make sure DMA requests triggered from EM2 are handled. |

| ID | Title/Problem | Effect | Fix/Workaround |
|-------|------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | The debugger cannot access the system when processing DMA request from EM2. | DMA controller, the system will keep waiting for it while denying debug access. | |
| ETM1 | ETM Trace Clock ETM Trace Clock needs to be delayed. | ETM trace clock is out of phase making the data transition occur at the same time as the ETM trace clock transitions. | ETM trace clock needs to be delayed between 10 ns and 1/4 of the trace clock period. |
| GPIO1 | GPIO wakeup from EM4 On GPIO wakeup from EM4 all cause bits for high-polarity wakeup pins are set. | All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup. | Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup. |
| LES1 | LESENSE and Schmitt trigger Schmitt trigger cannot be disabled on pins used for sensor excitation. | When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between VDD and VSS, the Schmitt trigger may consume a considerable amount of current. | Keep the input voltage close to VDD or VSS when LESENSE is not interacting with the connected sensor. |
| LES2 | LESENSE and DAC CH1 configuration DACCH0CONV in LESENSE_PERCTRL cannot be set to DISABLE if DAC CH1 is to be used. | LESENSE cannot control the DAC CH1 properly. | Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE. This enables DAC CH1 to be controlled properly, and it does not have any other effects as long as DACCH0OUT in LESENSE_PERCTRL is set to DISABLE. |
| LES3 | AUXHFRCO and LESENSE LESENSE will not work properly at low AUXHFRCO frequencies. | LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band. | Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE. |
| MSC1 | Prefetch unreliable Prefetch unreliable. | When prefetch is enabled, i.e. PREFETCH is set in MSC_READCTRL, wrong instruction data can be prefetched causing system failure. | Do not use prefetch. |
| OPA1 | Opamp 2 startup rampup When OPA2 is started the output rampup is constant independent of bias setting. | When OPA2 is started the output rampup is constant independent of bias setting. | No known workaround. |
| PRS1 | Edge detect on GPIO/ACMP | When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed. | Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC. |

| ID | Title/Problem | Effect | Fix/Workaround |
|--------|------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------|
| | Edge detect on peripherals with asynchronous edges might be missed. | | |
| USART1 | USART AUTOTX continues to transmit even with full RX buffer USART AUTOTX continues to transmit even with full RX buffer. | When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time. | No known workaround. |
| USB1 | USB DMA transfers with prescaled HFCLK USB DMA transfers to flash fail when prescaling HFCLK. | USB DMA transfers to flash may fail when prescaling HFCLK. | Do not prescale HFCLK when using USB-DMA transfers to read from flash. |
| USB2 | USB datalines USB datalines rise and fall time are slightly outside specification. | USB datalines rise and fall time are slightly outside specification under worst case conditions. They may fail USB certification eye test depending on PCB layout. | No known workaround. |
| USB3 | HNP Sequence fails if A-Device connects after 3.4ms HNP Sequence fails if A-Device connects after 3.4ms. | The B-Device core waits for less amount of time (3.4ms) and signals HNP fail and reverts back to Peripheral. HNP sequence fails if A-Device connects after 3.4ms. | No known workaround. |
| USB4 | USB A-Device delays the HNP switch back process Disconnecting the D+ lines only occur after 200ms, making the HNP switch back delayed. | The A-Device core delays the HNP switch back process. As per the USB-OTG 2.0 specification, the B-Device on the other side of USB either should wait for disconnect from A-Device or should switch to Peripheral mode and wait for A-Device to issue reset. Hence, there is no significant impact on actual operation. | No known workaround. |
| USB5 | B-Device as Host driving K-J pairs during reset A-Device misinterprets the K-J pairs as Suspend, after switching to High Speed mode. | If B-Device as Host on the other side of USB drives K-J pairs for more than 200ms during USB reset, the A-Device core exits peripheral state causing HNP process to fail. There is no significant impact since normally the host drives USB reset for lesser time than 200ms. | No known workaround. |
| USB6 | USB interrupts USB interrupts have changed from being level triggered to edge triggered. | USB interrupts are now triggered by signal edge rather than signal level. | Make sure to handle edge triggered interrupt, rather than signal level interrupts. |
| USB7 | Entry to EM4 causes temporary leakage from VREG0 | On transition from EM0 to EM4 a current leakage from VREG0 of up to 1 mA lasting a few seconds can occur. | No known workaround. |

| ID | Title/Problem | Effect | Fix/Workaround |
|------|-------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| | Entry to EM4 causes temporary leakage from VREGO. | | |
| USB8 | <p>Floating DM/DP pins cause leakage when USB is disabled</p> <p>Floating DM/DP pins cause leakage when USB is disabled.</p> | When the USB_DM or USB_DP pins are floating while the USB PHY is disabled, a current in the order of a couple hundred uA may leak from USB_VREGO to VSS. This will not be an issue if there is no voltage applied to USB_VREGO, either externally or through the USB regulator. | If there is no intention to use the USB module, e.g. the USB PHY is disabled, but there is still a voltage on USB_VREGO, make sure the USB_DM and USB_DP pins are defined. This can be done using GPIO or by defining them externally. |

2 Revision History

2.1 Revision 0.30

April 24th, 2012

Added BU6.

Added CMU4.

Added CMU5.

Added LES3.

Updated CMU3.

2.2 Revision 0.10

January 9th, 2012

Initial preliminary release.

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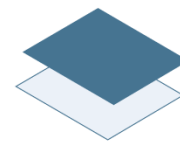
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