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EFM32TG840 Errata, Chip rev. B

F32/F16/F8



This document describes errata for the latest revision of EFM32TG840 devices.

1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p1 (www.arm.com) also applies to this device.

1.1 Chip revision B

Table 1.1. Erratas

ID	Title/Problem	Effect	Fix/Workaround
CMU1	LFxCLKEN write First write to LFxCLKEN can be missed.	For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACTKEN/LFB-CLKEN, may cause the write to miss its effect.	For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACTKEN/LFB-CLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
CMU2	LFXO configuration incorrect LFXO configuration incorrect.	For devices with PROD_REV < 15, the default value for LFXO-BOOST in CMU_CTRL are wrong.	On devices with PROD_REV < 15, change LFXOBOOST to 0.
EMU1	Debug unavailable during DMA processing from EM2 The debugger cannot access the system processing DMA request from EM2.	DMA requests from LESENSE and the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.	Make sure DMA requests triggered from EM2 are handled.
GPIO1	GPIO wakeup from EM4 On GPIO wakeup from EM4 all cause bits for high-polarity wakeup pins are set.	All EM4 wakeup cause bits for EM4 wakeup pins with high polarity are set on wakeup.	Use low polarity if possible. For active high, slow changing inputs, a solution is to sample the inputs on wakeup.
LES1	LESENSE and Schmitt trigger Schmitt trigger cannot be disabled on pins used for sensor excitation	When using LESENSE to excite a pin, the pin has to be configured in push-pull mode, which also enables the Schmitt trigger. If this pin has an input voltage somewhere in between 0.3*VDD and 0.7*VDD, the Schmitt trigger will consume a considerable amount of current.	Keep the input voltage to pins configured as push-pull outside the range 0.3*VDD to 0.7*VDD when LESENSE is not interacting with the connected sensor.
LES2	LESENSE and DAC CH1 configuration	LESENSE control of DAC CH1 cannot be enabled if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.	Configure DACCH0CONV in LESENSE_PERCTRL to anything but DISABLE, this enables DAC CH1 to be controlled properly. If DAC CH0 is not to be used, set DACCH0OUT in

ID	Title/Problem	Effect	Fix/Workaround
	LESENSE cannot control DAC CH1 if DACCH0CONV in LESENSE_PERCTRL is set to DISABLE.		LESENSE_PERCTRL to DISABLE. This will disable LESENSE control of DAC CH0, but still allow LESENSE to control DAC CH1.
LES3	AUXHFRCO and LESENSE LESENSE will not work properly at low AUXHFRCO frequencies.	LESENSE will not work properly when used with the AUXHFRCO running at the 1 or 7 MHz band.	Do not use a AUXHFRCO frequency band of 1 or 7 MHz when used in combination with LESENSE.
PRS1	Edge detect on GPIO/ACMP Edge detect on peripherals with asynchronous edges might be missed.	When using edge detect in PRS on signals from ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC edges can be missed.	Do not use edge detect on ACMP, GPIO, RTC, LETIMER, LESENSE, VCMP and BURTC.
USART1	USART AUTOTX continues to transmit even with full RX buffer USART AUTOTX continues to transmit even with full RX buffer.	When AUTOTX in USARTn_CTRL or AUTOTXEN in USARTn_TRIGCTRL is set, the USART will continue to transmit data even after the RX buffer is full. This may cause the RX buffer to overflow if the data is not read out in time.	No known workaround.
WDOG1	WDOG EM2 detection with LFXO digital/sine input The WDOG will mistake EM2 for EM3 if using LFXO with digital or sine input	When the WDOG is using LFXO with digital or sine input as a clock source, it will mistake EM2 for EM3. The EM2RUN and EM3RUN bits of WDOG_CTRL will behave accordingly.	When using LFXO with digital/sine input, EM3RUN must be set to keep the WDOG running in EM2.

2 Revision History

2.1 Revision 0.70

April 24th, 2012

Added LES3.

2.2 Revision 0.60

January 20th, 2012

Added GPIO1.

2.3 Revision 0.50

January 13th, 2012

Added USART1.

2.4 Revision 0.40

January 11th, 2011

Added CMU2.

Updated CMU1.

2.5 Revision 0.30

November 11th, 2011

Added CMU1.

Added PRS1.

2.6 Revision 0.10

May 20th, 2011

Initial preliminary release.

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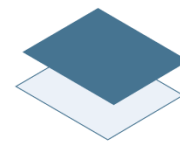
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