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EFM32G200 Errata, Chip rev C

F64/F32/F16

This document describes errata for the latest revision of EFM32G200 devices.

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1 Errata

This document contains information on the errata of the latest revision of this device. For errata on older revisions, please refer to the errata history for the device. The device datasheet explains how to identify chip revision, either from package marking or electronically.

In addition to the errata noted below, the errata for the ARM Cortex-M3 r2p0 (www.arm.com) also applies to this device.

1.1 Chip revision C

Table 1.1. Erratas

ID	Title/Problem	Effect	Fix/Workaround
ADC15	**Incorrect ADC Temperature Sensor Calibration Data** The ADC temperature sensor calibration value stored in the DI page is not correct.	Devices with PROD_REV values of 9 or 10 does not have correct ADC temperature sensor reading stored in the ADC0_TEMP_0_READ_1V25 register of the Device Information Page, and using this value for calculating the temperature will yield wrong results.	Instead of using the value stored in the Device Information table, use ADC0_TEMP_0_READ_1V25 = 0x906 and CAL_TEMP_0 = 0x19 when calculating the temperature. These values are gathered from production data, and will give an accuracy where 3x the standard deviation correspond to 5.2 degrees celsius.
CMU6	**LFXO Digital External Mode** LFXO ready flags are never set when LFXO is configured in Digital External Clock mode.	When LFXOMODE in CMU_CTRL is set to DIGEXTCLK the LFXORDY flag in CMU_STATUS and CMU_IF will not be set when the number of cycles set in LFXOTIMEOUT in CMU_CTRL has elapsed. Thus polling of this flag will not work. However, the clock propagates as normal. It is only the flag that is not set.	To detect that the clock has propagated through the ripple counter, write to any Asynchronous Register in any Low Energy peripheral and wait for SYNCBUSY for that register field to go low. Remember to enable the LE core clock and the clock for the LE peripheral you choose. For example, write 0xA5 to RTC_COMP0 and wait for COMP0 in RTC_SYNCBUSY to go low.
CMU8	**LFxCLKEN write** First write to LFxCLKEN can be missed.	For devices with PROD_REV < 15, enabling the clock for LFA/LFB after reset and then immediately writing LFACLKEN/LFBCLKEN, may cause the write to miss its effect.	For devices with PROD_REV < 15, make sure CMU_SYNCBUSY is not set before writing LFACLKEN/LFBCLKEN. Can temporarily switch to HFCORECLKLEDIV2 to speed up clearing synchbusy.
CMU9	**LFXO configuration incorrect** LFXO configuration incorrect.	For devices with PROD_REV < 15, the default value for LFXOBOOST in CMU_CTRL are wrong.	On devices with PROD_REV < 15, change LFXOBOOST to 0.
EMU3	**EM4 current** In EM4 the device may consume 700nA instead of 20nA.	If EM4 is issued within a 10µs-12µs window after the 1kHz RC oscillator rising edge transition the device will permanently consume 700nA.	There two possible workarounds for this issue. The first workaround is using the WDOG to identify the rising edge transition and add a delay before going into EM4. Write on the WDOG_CTRL register (for instance WDOG->CTRL|=WDOG_CTRL_CLKSEL_ULFRCO) and wait for the SYNCBUSY to be released. The release of the SYNCBUSY happens on a rising edge transition of the 1Khz clock. After

ID	Title/Problem	Effect	Fix/Workaround
			that insert a number of __NOP(); to cause a delay of 20µs (12µs plus margin). The number of __NOP(); will depend on the processor frequency. After the delay EM4 can be entered safely. Note: to implement this workaround the WDOG can not be locked, otherwise the registers will not be written. The second workaround is by outputting the ULFRCO on a pin (CMU_CLK0) using CMU_CTRL and CMU_ROUTE registers. That pin should then be configured as push pull with interrupt enable on rising edge, so the device can go to EM2 while it waits for the ULFRCO rising edge transition. When the interrupt occurs clear it and add a number of __NOP(); before entering EM4, as described in the first workaround. Note: the pin used to output the ULFRCO should be driven by an external source.
EMU4	**Sequencing of Analog and Digital Power** Power-on Reset might fail if power is applied to IOVDD_x or VDD_DREG before AVDD_x	The device might lock up if power is applied to IOVDD_x or VDD_DREG pins before AVDD_x pins during power up. This lock-up state can be exited by removing power to the device followed by a power up sequence according to what is described in the workaround.	Make sure that the power on the AVDD_x pins ramp earlier or at the same time as the power on IOVDD_x and VDD_DREG during power up. Practical schematic recommendations for this workaround are given in the EFM32 Application Note "AN0002 Hardware Design Considerations".
EMU5	**Debug unavailable during DMA processing from EM2** The debugger cannot access the system processing DMA request from EM2.	DMA requests from the LEUART can trigger a DMA operation from EM2. While waiting for the DMA to fetch data from the respective peripheral, the debugger cannot access the system. If such a DMA request is not handled by the DMA controller, the system will keep waiting for it while denying debug access.	Make sure DMA requests triggered from EM2 are handled.
EMU6	**SWO line pulled low in EM2** SWO pulled low in EM2.	The SWO line is pulled low in EM2. This can be interpreted as garbage by an outside observer.	Before entering EM2, disable pin-enable by clearing SWOPEN in GPIO_ROUTE, and set SWO pin output high. After exiting EM2, the SWO pin should be re-enabled.
RTC1	**RTC PRS output** The RTC PRS output might cause false triggers	If the RTC is selected as a PRS producer there might occur glitches which will accidentally cause false triggers.	Do not use the RTC as a PRS producer, instead use one of the other timer sources (e.g. TIMER0).
USART1	**U(S)ART Double Buffer** Transmission control through TXDATAX and TXDOUBLEX does not work with data double buffering.	When a frame is loaded into the transmission shift register, transmission control bits are always taken from outer buffer element. If only one frame is in the U(S)ART buffer, the content of the buffer elements is equivalent, and transmission control bits work as specified. If two frames are in the buffer however, the control bits for the frame in the outer buffer are used for transmitting the frame in inner buffer. This is not a problem for	If using transmission control bits in registers TXDATAX or TXDOUBLEX make sure there are not more than one frame in the U(S)ART buffer at a time, or that the control bits are equal. When TXBL in U(S)ARTn_CTRL is cleared, the TXBL status and interrupt flags in U(S)ARTn_STATUS and U(S)ARTn_IF respectively tell when the buffer is empty. When using trans-

ID	Title/Problem	Effect	Fix/Workaround
		frames consisting of more than 9 bits, since these large frames occupy both the inner and outer buffer elements.	mission control bits, a single frame can then be loaded into the USART for transmission.
WDOG2	**WDOG does not freeze in EM2/EM3** The WDOG keeps running in EM2 and EM3 even though EM2RUN and EM3RUN bits in WDOG_CTRL are programmed to 0.	If the WDOG is enabled when entering EM2 or EM3, a WDOG reset will occur unless the system wakes up from EM2/EM3 (by interrupt) and clears the WDOG timer before the WDOG times out.	Disable WDOG before entering EM2/EM3 by writing EN bit in WDOG_CTRL to 0. This requires that the WDOG configuration is unlocked (LOCK bit in WDOG_CTRL = 0). If WDOG configuration is locked, the WDOG will remain enabled in EM2/EM3 and the system must wake up the device from EM2/EM3 and clear WDOG before WDOG times out.
WDOG3	**WDOG EM2 detection with LFXO digital/sine input** The WDOG will mistake EM2 is EM3 if using LFXO with digital or sine input	When the WDOG is using LFXO with digital or sine input as a clock source, it will mistake EM2 for EM3. The EM2RUN and EM3RUN bits of WDOG_CTRL will behave accordingly.	When using LFXO with digital/sine input, EM3RUN must be set to keep the WDOG running in EM2.

2 Revision History

2.1 Revision 1.70

January 11th, 2011

Added CMU9.

Updated CMU8.

2.2 Revision 1.60

November 10th, 2011

Added CMU8.

Added EMU6.

2.3 Revision 1.50

May 20th, 2011

Added ADC15.

Added EMU5.

Added WDOG3.

2.4 Revision 1.40

November 17th, 2010

Added EMU4.

2.5 Revision 1.30

October 26th, 2010

Added EMU3 and RTC1.

2.6 Revision 1.20

August 31st, 2010

Removed Erratas not valid for chip revision C.

Added WDOG2.

2.7 Revision 1.10

June 25th, 2010

Removed ADC7, DAC6, and LCD3.

Added ACMP1, ADC12-ADC13, CMU6-CMU7, DAC7, LEUART3, LETIMER1, TIMER1, USART2-USART11, VCMP1-VCMP2.

2.8 Revision 1.00

April 23rd, 2010

Removed ADC_VCM errata.

Updated the erratas which are to be fixed in chip revision C.

2.9 Revision 0.10

April 8th, 2010

Initial preliminary release.

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Table of Contents

1. Errata 2
    1.1. Chip revision C 2
2. Revision History 5
    2.1. Revision 1.70 5
    2.2. Revision 1.60 5
    2.3. Revision 1.50 5
    2.4. Revision 1.40 5
    2.5. Revision 1.30 5
    2.6. Revision 1.20 6
    2.7. Revision 1.10 6
    2.8. Revision 1.00 6
    2.9. Revision 0.10 6
A. Disclaimer and Trademarks 7
    A.1. Disclaimer 7
    A.2. Trademark Information 7
B. Contact Information 8
    B.1. Energy Micro Corporate Headquarters 8
    B.2. Global Contacts 8

List of Tables

1.1. Erratas 2

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